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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,174	02/13/2004	Kenneth Koch II	10017911-3	4476

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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,174	KOCH ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,7-12,14,16-18 and 20-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14,16-18 and 22* is/are allowed.

6)☒ Claim(s) *1,3,7-12,25 and 26* is/are rejected.

7)☒ Claim(s) *20,21,23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Responses to Amendment

1. This office action is responsive to the amendment filed on 1/21/05.

Terminal Disclaimer

2. The terminal disclaimer filed on 1/21/05 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of any of U.S. Patent No. 6,759,880, U.S. Patent No. 6,753,708, or co-pending application 10/777,902 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Objections

3. Claims 20, 23 and 24 are objected to because of the following informalities:

Claim 20, line 12, "and first" should be changed to --and the first-- to avoid unclear antecedent basis (see line 6).

Claims 23 and 24 are objected to because they include the informality of claim 20.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3, 7-11 and 25-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Love (USP 5,068,553).

Note that Figure 3 of Love discloses a circuit which includes a first terminal (IN); a driver (86, 88) having a first transistor (PFET 86) and a second transistor (NFEF 88); output terminal (OUT); pulse shaping circuitry (68, 72, 70 and 80) comprising a resistive element (resistor 72), a capacitor (NFET 80) and a switching circuitry (68, 72, 70) comprising an inverter (68, 72, 70) wherein the inverter comprises the resistive element (resistor 72), a PFET (68) and an NFET (70). Note that because the PFET and NFET transistors having opposite conductivity so the on/off of transistors 86 and 88 in Figure 3 must be opposite to each other, i.e., transistors 86 and 88 are not ON simultaneously (i.e., when input IN is Hi then node 76 is Lo, then transistor 86 is ON so the source-drain path of transistor 86 is ON, while transistor 88 is OFF which is the source-drain path of the transistor 88 is OFF; and vice versa, when input IN is LO, so node 76 is Hi, then source-drain path of transistor 86 is OFF while source-drain path of transistor 88 is ON). Note that for claim 20, the first transistor (either transistor 86 or transistor 88), the second transistor (68) the third transistor (70). Thus, because the structure of the claims are fully met so all the functional limitations of the claims are also met (MPEP 2114; In re Swinehart, 169 USPQ 226 (CCPA 1971); and In re Schreiber, 44 USPQ2d 1429 (Fed. Cir. 1997)).

Claim Rejections – 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 3, 7-12 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamasaki et al. (USP 5,694,065) in view of Rapp (USP 5,280,420).

With respect to claims 1, 3, 7-12 and 25, Figure 2 of the Hamasaki et al. reference discloses a circuit which includes a first terminal (IN); a driver (50, 60) having a first transistor (PFET 50) and a second transistor (NFEF 60); output terminal (OUT); pulse shaping circuitry (72, 74, Rn, Cn, 82, 84, Rp and Cp) comprising a resistive element (resistor Rn), a capacitor (Cn) and a switching circuitry (72, 74) comprising an inverter (72, 74, Rn. Note that, for broadest reasonable interpretation, the combination of elements 72, 74 and Rn forms an inverter, i.e., the output of inverter is signal D01) wherein the inverter comprises the resistive element (resistor 72), a PFET (72) and an NFET (74). Figure 2 of the Hamasaki et al. reference does not disclose that the first capacitor (Cn) comprising a field effect device having a conductivity type opposite to the conductivity type of the first transistor (PFET 50). However, the Rapp reference discloses that a capacitor is easily formed by using an NMOS transistor that has its drain and its source connected together (lines 10-16 and lines 61-63 of Col. 7). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 2 of the Hamasaki reference to use specific capacitor-connected NMOS transistor (as taught by the by the Rapp reference) for broad capacitor elements in the circuit of Figure 2 of the Hamasaki reference (i.e., each of the capacitors Cn and Cp in Figure 2 is implemented by a capacitor-connected NMOS transistor) for the purpose of more efficiently implementation in silicon (i.e., easily integrated by connection the source and drain of the NMOS together) and therefore the operation of the circuitry would be more efficiency since the circuit is fully integrated. Thus, this modification meets all the limitations of this claim including the "first

capacitor comprising a field effect device having a conductivity type opposite to the conductivity type of said one of said transistors" because the capacitor Cn in this modification comprising an NMOS device (capacitor-connected NMOS transistor) having the conductivity opposite to the PMOS transistor (50). Note that all the functional limitations in this claim are also met because the structure of the claim is fully met as discussed above.

Allowable Subject Matter

8. Claims 14, 16-18 and 20-23 presently would be allowed. Note that claims 20, 21 and 23 would only be allowed if amend to overcome the informality set forth above.

9. Claim 24 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

10. Applicant's arguments filed 1/21/05 have been fully considered but they are not persuasive.

With respect to the Love reference, applicant argues that the Love reference does not disclose the capacitor comprising a field effect device having a conductivity type opposite to the conductivity type of the said one of said transistors. However, this argument is not persuasive Figure 3 of the Love reference shows the capacitor is n-channel MOSFET 80, the one of said transistors is p-channel 82 which has a conductivity of type opposite to the conductivity type of the capacitor n-channel 80.

With respect to the combination of the Love and the Rapp reference, applicant argues that there is no disclosure in Rapp of a capacitor connected between the gate electrode of a transistor

having a first conductivity type and a power supply terminal and a capacitor formed by an MOS device having a conductivity type opposite from the transistor the transistor. However, this argument is not persuasive because be Rapp reference is used as a secondary reference to support that a capacitor is easily formed by connecting the source and drain of an NMOS transistor together. Hence, when the connection of the source and drain of the NMOS transistor would be one terminal of the capacitor, while the gate of the NMOS transistor is the other terminal of the capacitor.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 4, 2005

LONG NGUYEN
PRIMARY EXAMINER